Yuqing YE

Embedded Systems & Hardware Engineering

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Summary of Qualifications

Embedded & Hardware: ESP32-S3, ESP-IDF, FreeRTOS, Arduino, I2S, GPIO, KiCad, FPGA

Languages: C/C++, Java, Python, SystemVerilog **Systems & Tools**: Linux, Git, CMake, SSH

AI/Compute: YOLO, model quantization, edge inference, SoC deployment

Education

University of Washington, Seattle Expected June *2028*

B.S. Electrical & Computer Engineering (ECE)

GPA: *3.97* **Relevant coursework:** *Programming & Data Structures, Digital Circuits & System* ***Planned:*** *Computer Architecture*

Relevant Experience (click to check my portfolio)

ARC Lab **Undergraduate Research Assistant,** 03/2026- Present

Explored efficient model deployment for drone vision systems under strict onboard resource constraints with a team of 7.

- Built and benchmarked an AI deployment pipeline for resource-constrained SoC platforms, evaluating model quantization and hardware-aware tradeoffs between inference accuracy and runtime performance.
- Benchmarked AMD Kria KV260 performance under real-time object detection workloads, evaluating OnSemi camera frame-capture latency and image quality alongside system power consumption. Coordinated closely with the model development team to align algorithm design with hardware limitations.
- Conducted model performance benchmarking using images, videos, and live camera inputs, achieving 70.21 mAP at 14–15 FPS on the SoC platform.
- Identified a substantial accuracy drop between RGB (65–70% mAP) and grayscale (30–40% mAP) datasets, supporting ongoing bottleneck analysis for robust edge workload.

Independent Project - Intelligent Robotic Pet **Embedded Systems Engineer,** 06/2026 - Present

Developed an intelligent dog with facial expression and capability of moving and talking, responsible for entertaining and accompanying people with stressful lifestyles.

- Integrated software components (LLM, STT/TTS) with ESP32-S3 peripherals including microphone, speaker, servos, and OLED through I2S, I2C, GPIO, Wi-Fi, and WebSocket interfaces.
- Integrated I2S audio peripherals, GPIO interfaces, and event-driven device control in C/C++ using ESP-IDF.
- Performed HW/SW boundary debugging on I2S slot configuration, sample rate, sensor IO, and firmware event flow.
- Diagnosed and resolved I2S audio pipeline issues, enabling end-to-end streaming from microphone input through STT, LLM inference, TTS, Opus decoding, and speaker output.

Halogen.AI **Software Engineer Intern**

06/2025- 08/2025

Built AI-powered Go-To-Market assistant to help small business founders with limited resources reduce decision fatigue.

- Diagnosed and resolved the output storage issue in the strategy generator, reducing output-display errors by 50%.
- Shipped prototype to beta users; outputs recognized by 3 prospective enterprise clients as consistent with their insights.

12/2025- 01/2026

- Shipped a plugin to help WordPress community with visibility issues in AI responses by generating AI readable files;
- Results recognized by manager and were later expanded to a full pipeline of AI Answer Engine Optimization.

UW-Social - Student-Based Event Searching & Recommendation Platform **Project Leader**, 03/2025-Present

Built event platform powered by AI to centralize event resources and lower the information barrier students face.

- Formed and led a 7-member cross-functional team (engineers, designers, marketers); Organized persistent product iteration based on feedback; Facilitated mutual growth among 200+ community members by encouraging event information and event notes sharing.
- Empowered 100 active users with 300+ quality-verified on-campus events and 20+ event notes.

Activities

High Performance Computing Conference 2025 (SC25) **Immersion Program,** 11/2025

- Leveraged Linux in performing simple Physics simulation with supercomputer Frontier; developed basic knowledge in parallel computing including SLURM schedulers and inter-node communications.
- Visited exhibitors including NVIDIA and IBM; studied the technical trend in AI infrastructure industry and Focused future interests in model's deployment on hardware systems.